



Procyon Platform

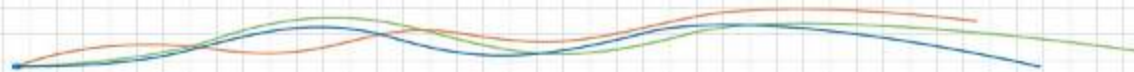
*The ultra-high-performance
simulation and control platform*



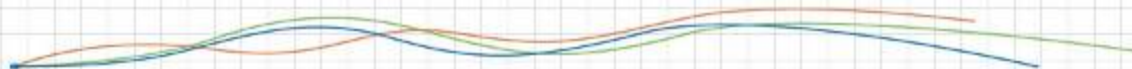
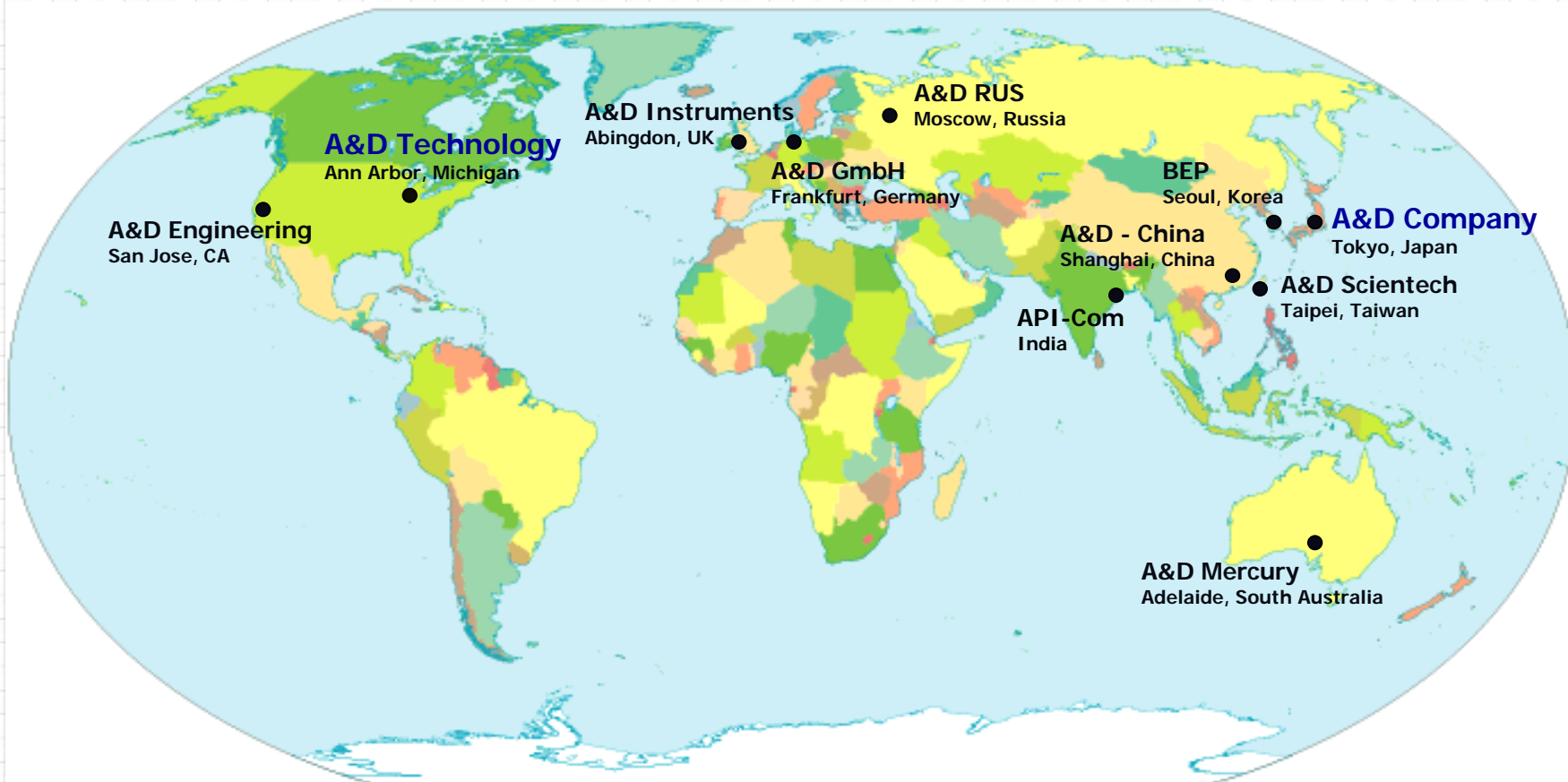
Introduction to A&D



- Headquarters in Tokyo, Japan
- Founded May, 1977
- Sales (FY07): US\$350 million
- Listed at TSE I: April, 2005
- Number of employees:
 - 2751 World Wide
 - 600 in Japan
 - 92 in Ann Arbor, MI

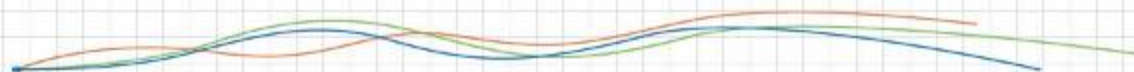
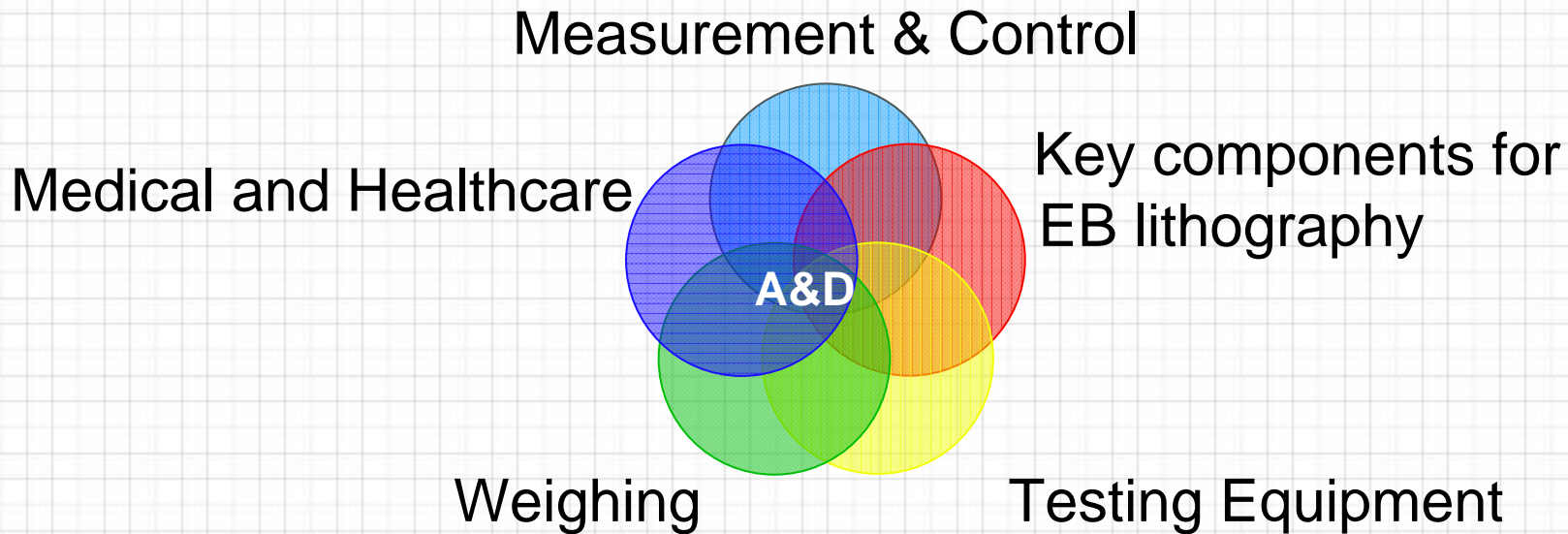


Global Presence





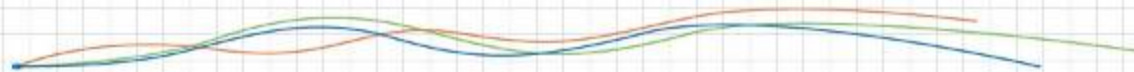
A&D Group



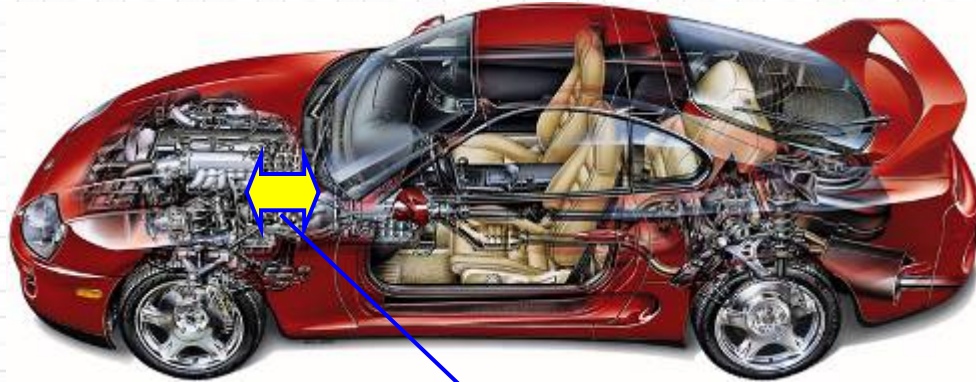
A&D Product Lines



- Weighing products
 - Analytical/Precision balances
- Medical products
 - Consumer/professional blood pressure monitors
- Testing equipment
 - Vibration and noise analysis software
 - FFT spectrum analysis
 - Universal tensile testing machines
- Electron beam-related systems
- Engine Test Cell Tools
 - Combustion Analysis
 - Automated Calibration Tools
 - Lab Management
- **DSP Systems**
 - **Real-time simulation systems**
 - **Measurement and control systems**
 - **Model-based development tools**
 - **Application: Automotive, Aircraft, Power Generation plant, Defense, etc.**



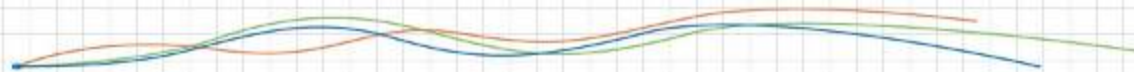
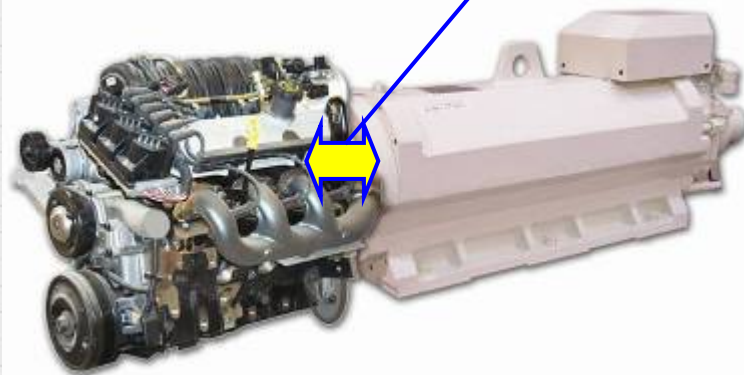
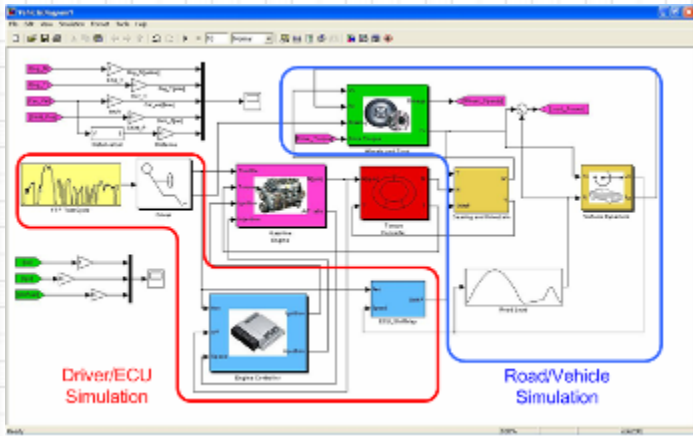
DSP Application Vehicle Simulation in the Test Cell



Real
World

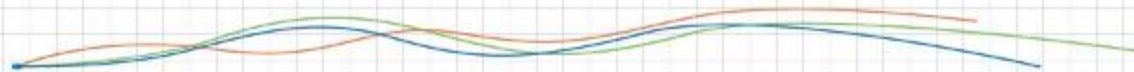
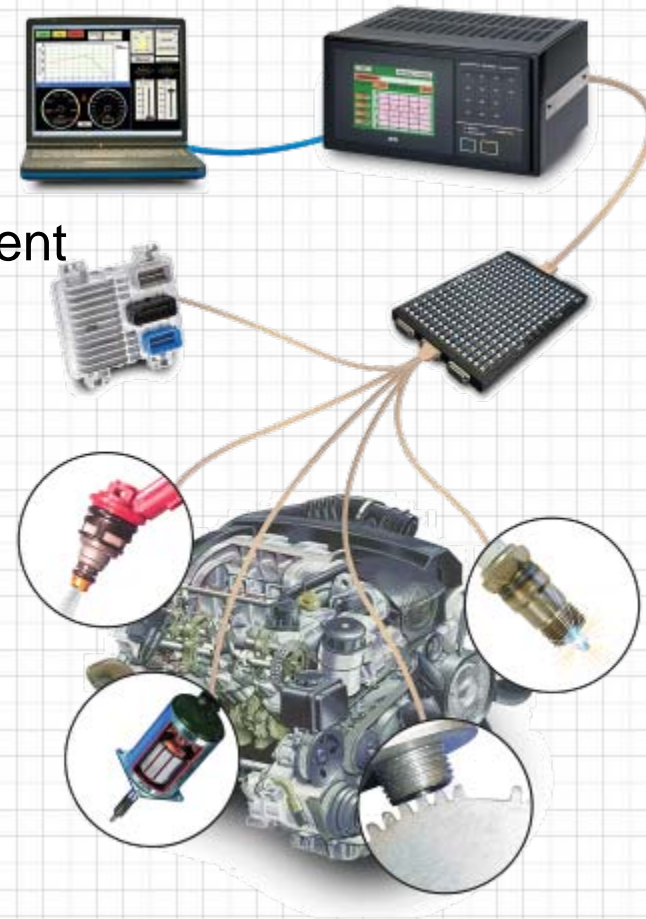
Speed/torque between engine and vehicle = Speed/torque
between engine and dyno

Engine in
the Loop
Vehicle
Simulation



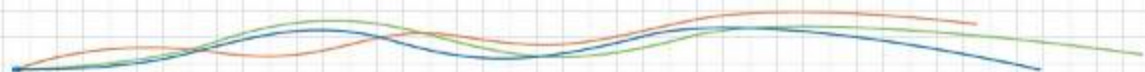


- Test cell specific
 - Tasks: competitive benchmarking, aftertreatment and catalyst testing/aging, engine mapping, transient studies, component testing/development, base calibration work, knock/misfire studies, etc.
- Customer motivation
 - Complete control over ECU
 - Flexible vs. fixed
 - Targeted applications
 - Expandable for future tests, control, I/O...





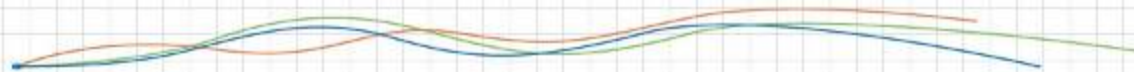
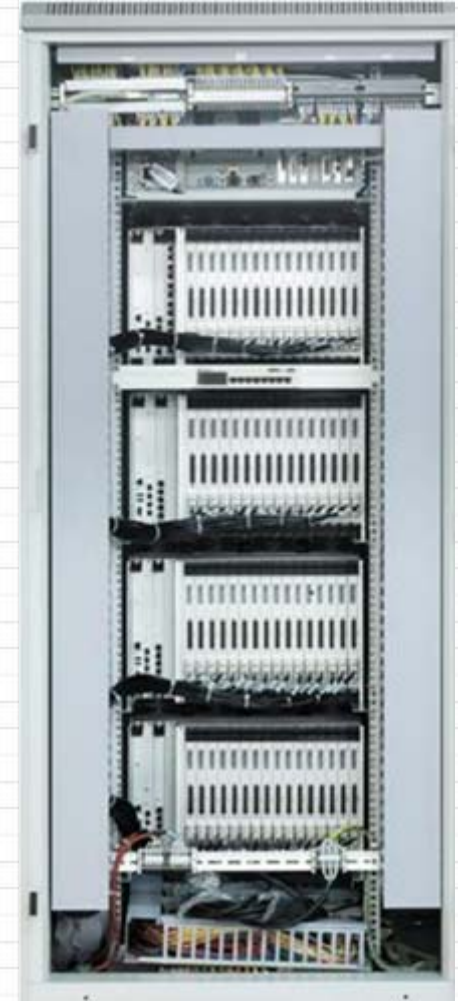
- Current platform Limitation
 - Single CPU for model execution
 - PCI base shared bus architecture
- Customer's requests for next generation platform
 - Larger models
 - Complicated model
 - Hybrid Vehicle, Aircraft, etc
 - Large number of I/O
 - Faster model cycles
 - Electrical simulation/control (ex. Motor simulation/control)
 - >100kHz Input-output loop





What is Procyon?

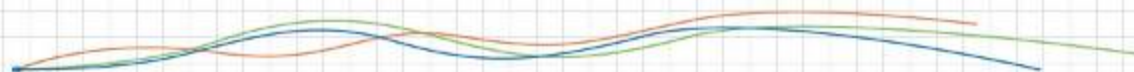
- Next generation DSP Platform
- Supports Multi-Core/Multi-CPU (max 32 CPU cores in one box)
- High Performance I/O Boards with HyperTransport and PCI Express
- User-programmable FPGA Co-Processors
- Support CompactPCI Standard Peripheral Boards
- Efficient Multi-Core/Multi-CPU Programming and Execution Environment with The Mathworks MATLAB/Simulink
- Open System



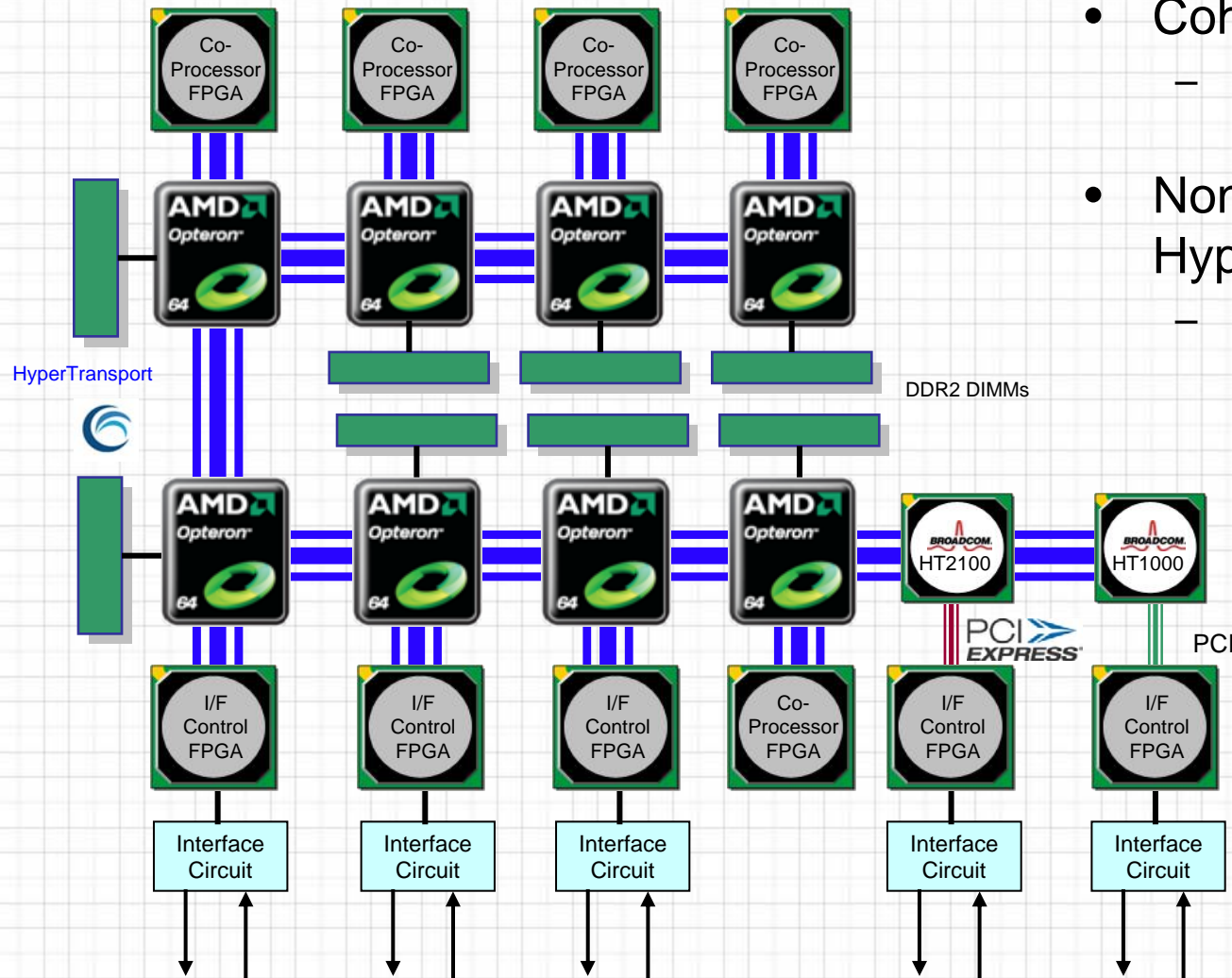
Why HyperTransport?



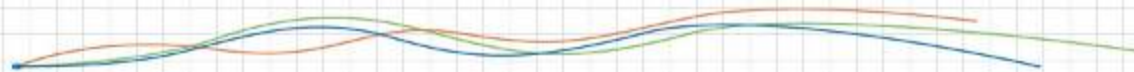
- Open Specification
 - Open HT core was available(University of Heidelberg)
- High performance
 - Low Latency I/O
 - Direct I/O connect architecture to AMD Opteron
 - High speed and wide bandwidth interface
 - Bi-directional high speed interface
 - » HT200, 16bit 1.6GByte/s for I/O interface
 - » HT1000, 16bit 8GByte/s for CPU-CPU connection
- Flexible Configuration
 - Add Opteron CPU or I/O interface



Procyon System Internal Architecture

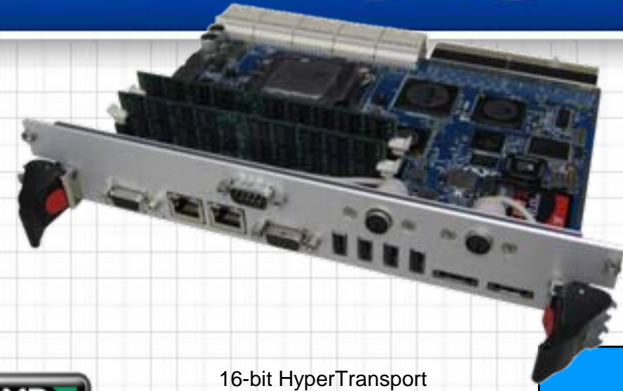


- Coherent HyperTransport
 - AMD Opteron Quad Core x 8 = 32 Core System
- Non-Coherent HyperTransport
 - Low Latency Direct I/O Connection to CPU

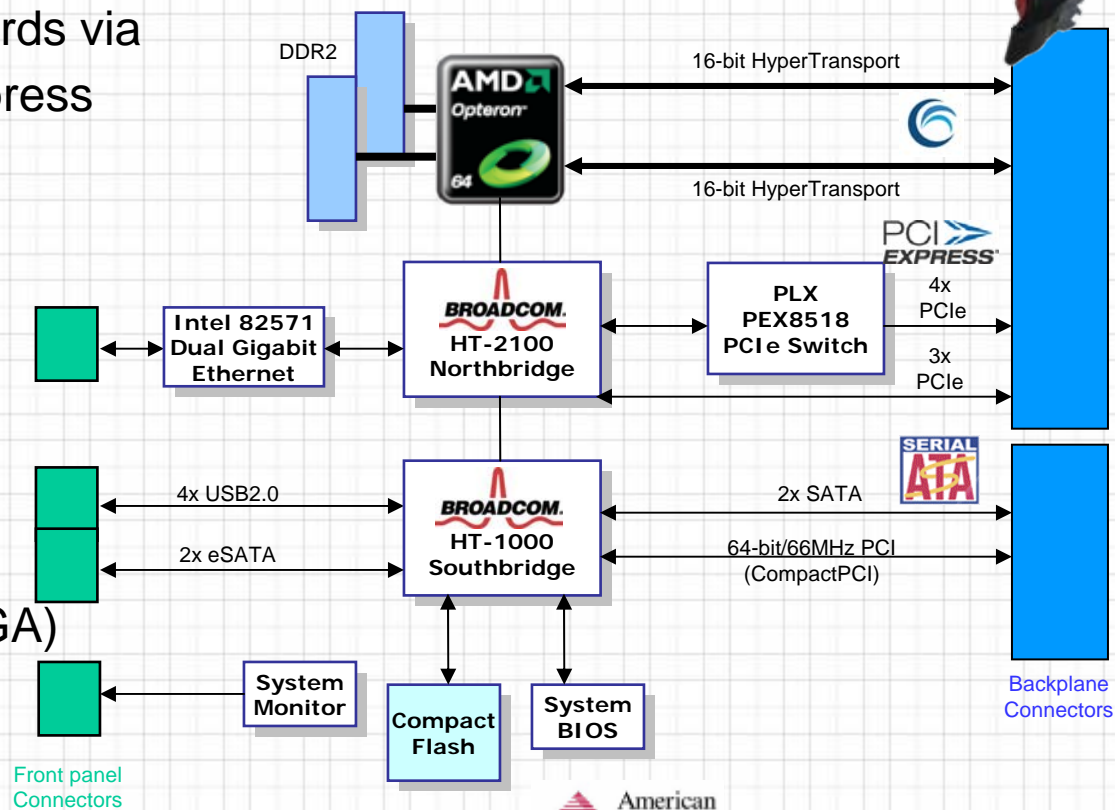


Castor

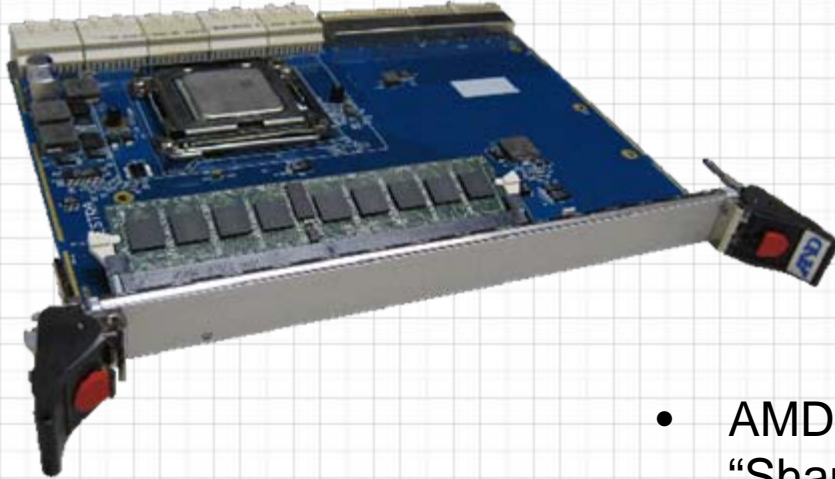
AD7003 Procyon System SBC



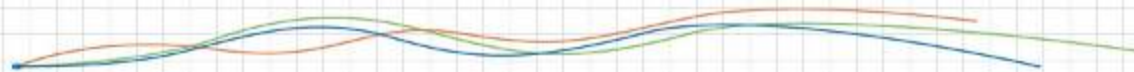
- AMD Opteron™ (supports Quad-Core “Shanghai” processor family)
- Broadcom HT2100/HT1000 Chipset
- Connects to peripheral boards via HyperTransport or PCI Express
- DDR2 DIMM x 2
- Gigabit Ethernet x 2
- USB2.0 x 4
- VGA
- SATA and eSATA
- System monitor function
- AMI BIOS (supports ncHT & cHT FPGA)
- Supports CompactPCI peripheral boards



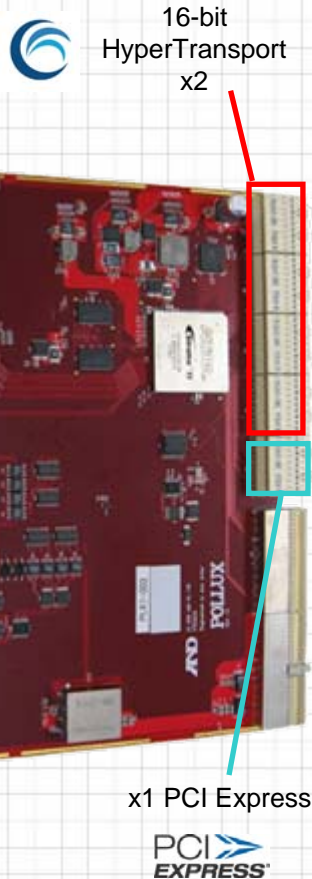
American Megatrends



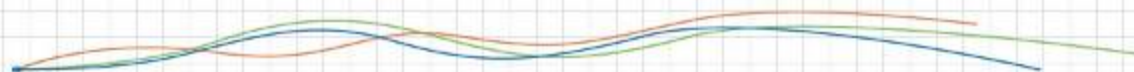
- AMD Opteron™ (supports Quad-Core “Shanghai” processor family)
- DDR2 DIMM
- HyperTransport Interfaces
 - 2x 16-bit bi-directional
 - 1x 8-bit bi-directional



Pollux: Interface Evaluation Board



- Interfaces:
 - HyperTransport
 - 2x 16-bit bi-directional HyperTransport links
 - HT Core with HT200 and 16bit wide links with University of Heidelberg HyperTransport core
 - PCI Express
 - x1 [single lane] configuration
- I/O
 - Magnetically Isolated I/O
 - 8 in, 8 out
 - Logic Analyzer Connection
 - 32 data, 2 clocks
- FPGA
 - Altera Stratix II
 - Standard build: 60k LUT, speed grade 3 (fastest)
 - Custom build: up to 180k LUT





Supports 3 types of Interconnections:

- **HyperTransport**

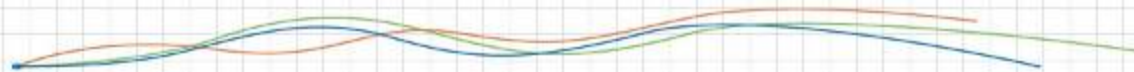
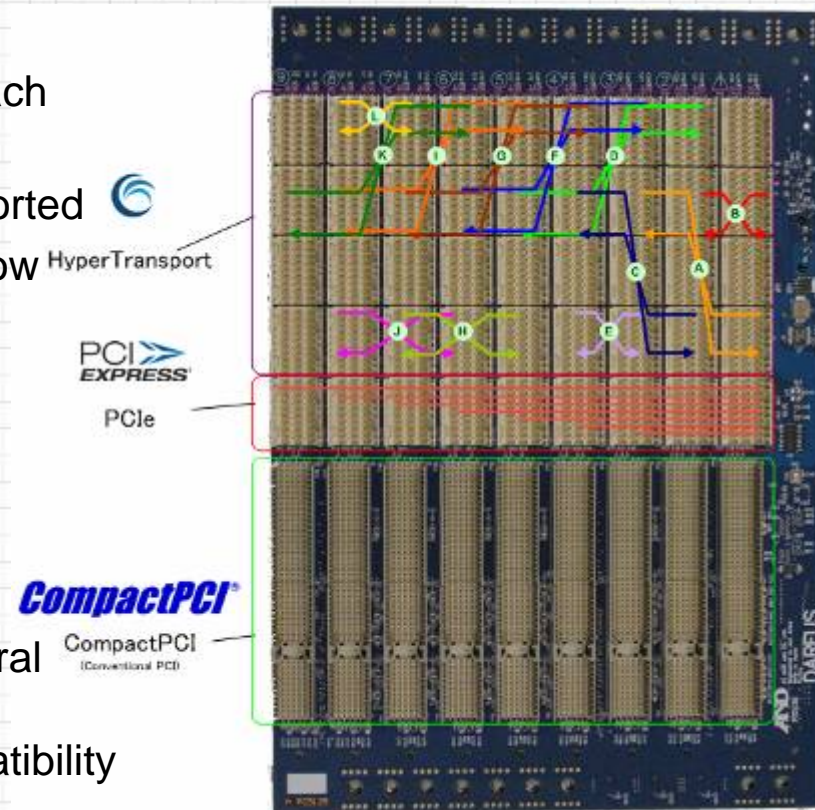
- High speed point-to-point communication
- 16 Bits x 1000 MHz x 2 transfers/clock x 2 (each direction) = 64 Gbit/s
- Multi-CPU environment; max 8 CPUs supported
- Direct connect I/O interface to CPU → Low latency I/O

- **PCI Express**

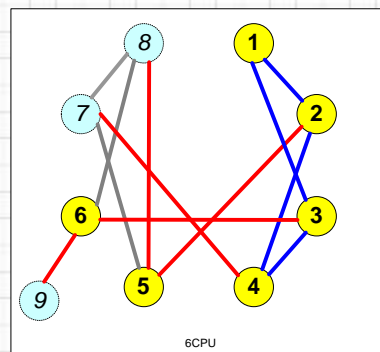
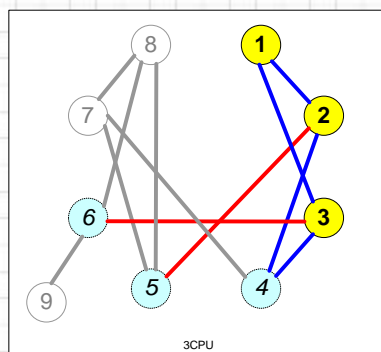
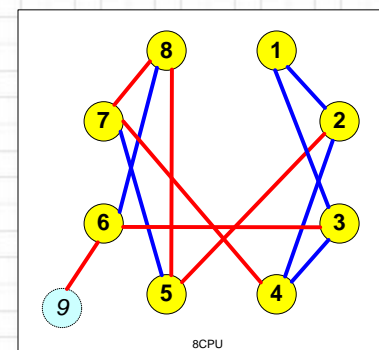
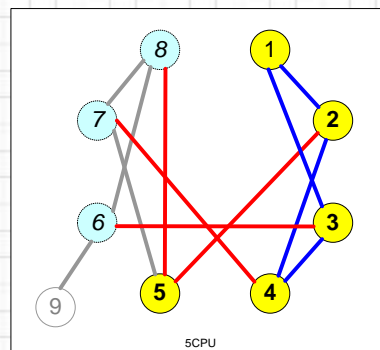
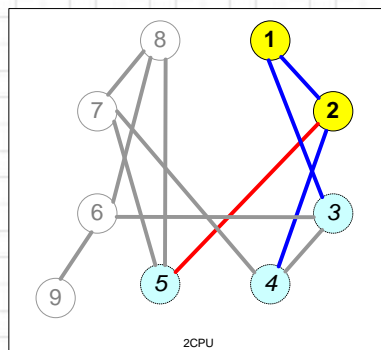
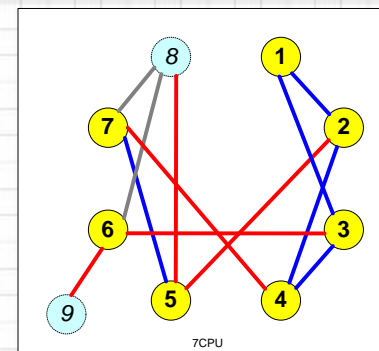
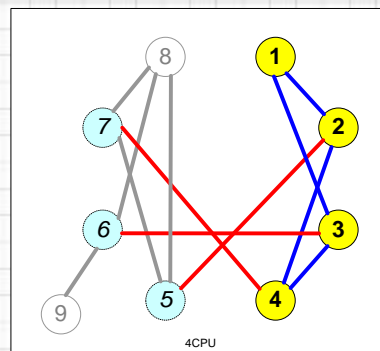
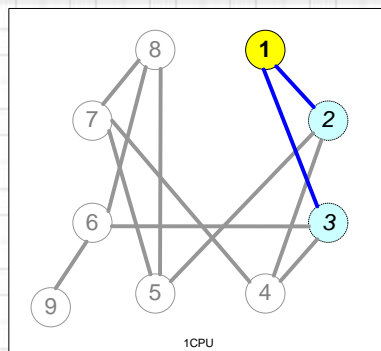
- x1 [single lane] configuration

- **Conventional PCI**

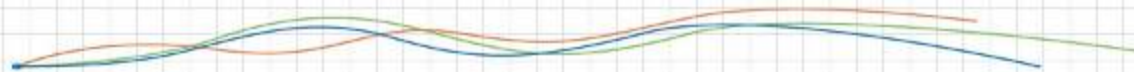
- 64bit/33MHz
- Supports off-the-shelf CompactPCI peripheral boards
- A&D specific extension for backward compatibility for A&D boards



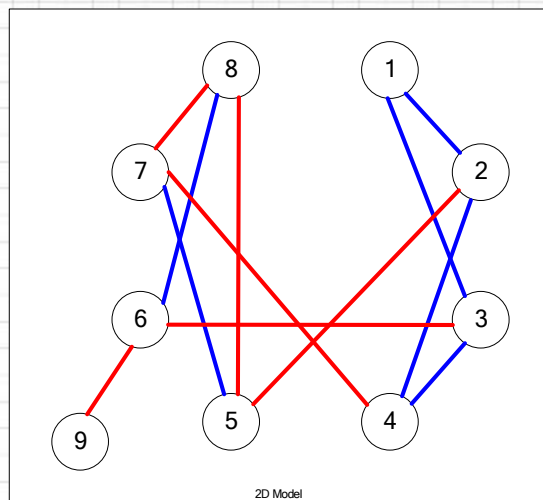
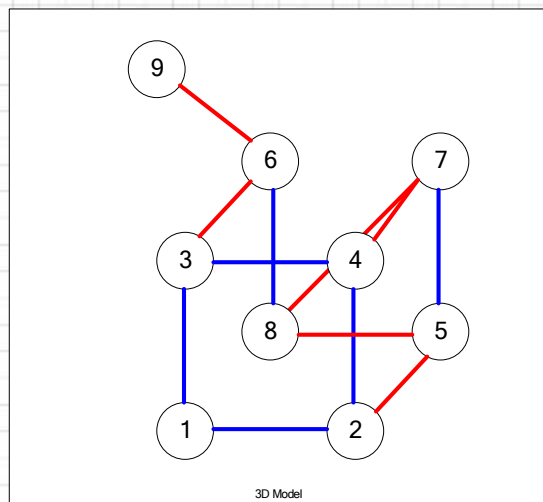
40HP Procyon System Backplane Configuration Options



- CPU
- I/O or FPGA Co-Proc Board
- 16bits, 1GHz
- 8bits, 800MHz
- Unused Link

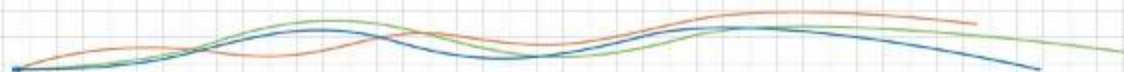


40HP Procyon System Backplane Internal Connection



Node	Node	#Hop	Num of 8bit/800M Hz Link	Node	Node	#Hop	Num of 8bit/800M Hz Link	
1	2	1	0	4	5	2	1	
	3	1	0		6	2	1	
	4	2	0		7	1	1	
	5	2	1		8	2	1	
	6	2	1		9	3	2	
	7	3	1		6	2	1	
	8	3	1		7	1	1	
	9	3	2		8	1	1	
	3	2	0		9	3	2	
2	4	1	0	6	7	2	2	
	5	1	1		8	1	1	
	6	3	1		9	1	1	
	7	2	1		8	1	1	
	8	2	2		9	3	2	
	9	4	2		8	9	2	1
	4	1	0					
	5	3	1					
	6	1	1					
3	7	2	1					
	8	2	1					
	9	2	2					

— 16bits, 1GHz
— 8bits, 800MHz



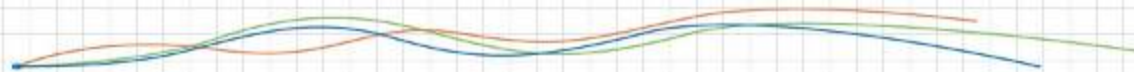
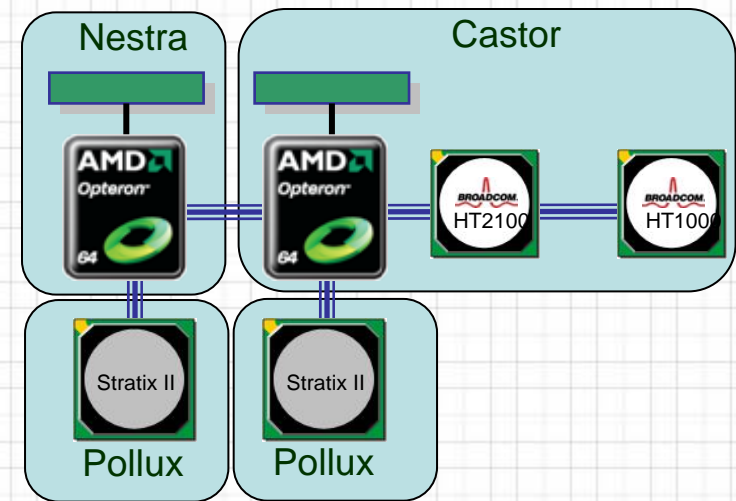


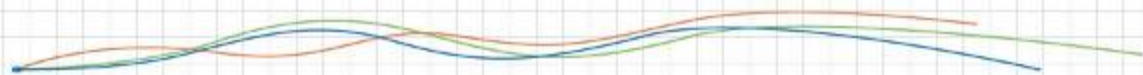
- **Hardware Environment**

- Dareus
 - 9 slot Backplane
- Castor (AD7003)
 - Quad-Core AMD Opteron 8378 (Shanghai)
 - 2x 1GB DDR2 800 DRAM
- Nestra (AD7003-01)
 - Quad-Core AMD Opteron 8378 (Shanghai)
 - 1GB DDR2 800 DRAM
- 2 x Pollux
- Backplane Configuration
 - Castor – Nestra – Pollux – Pollux

- **Software Environment**

- Linux Kernel 2.6.26.7
 - 64bit/NUMA Configuration
- Xenomai 2.4.6.1





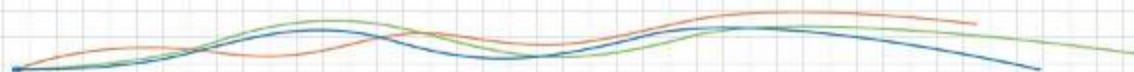


• Benchmark Result

– Can achieve **2us (500kHz) I/O loop**

- With CPU calculation
 - 750ns for Nestra
- With 256Byte bi-directional DMA
- With System Stress (Memory access, HDD access, Ethernet Transaction, ...)
 - Current Generation system I/O loop is 50us (20kHz)

System Stress	Step Size	Model Execution time	
		Castor	Nestra
N	2us	800ns	800ns
Y	2us	350ns	750ns
N	3us	1800ns	1800ns
Y	3us	1200ns	1750ns





Stanford Pervasive Parallelism Laboratory

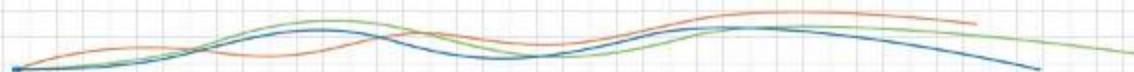
- Goal: researching the parallel computing platform for 2012
- Director: Kunle Olukotun
- Involves architecture, algorithms, programming models

Research Methodology



- **Conventional approaches are still useful**
 - Develop app & SW system on existing platforms
 - Multi-core, accelerators, clusters, ...
 - Simulate novel HW mechanisms
- **Need some method that bridges HW & SW research**
 - Makes new HW features available for SW research
 - Does not compromise HW speed, SW features, or scale
 - Allows for full-system prototypes
 - Needed for research, convincing for industry, exciting for students
- **Approach: commodity chips + FPGAs in memory system**
 - Commodity chips: fast system with rich SW environment
 - FPGAs: prototyping platform for new HW features
 - Scale through cluster arrangement

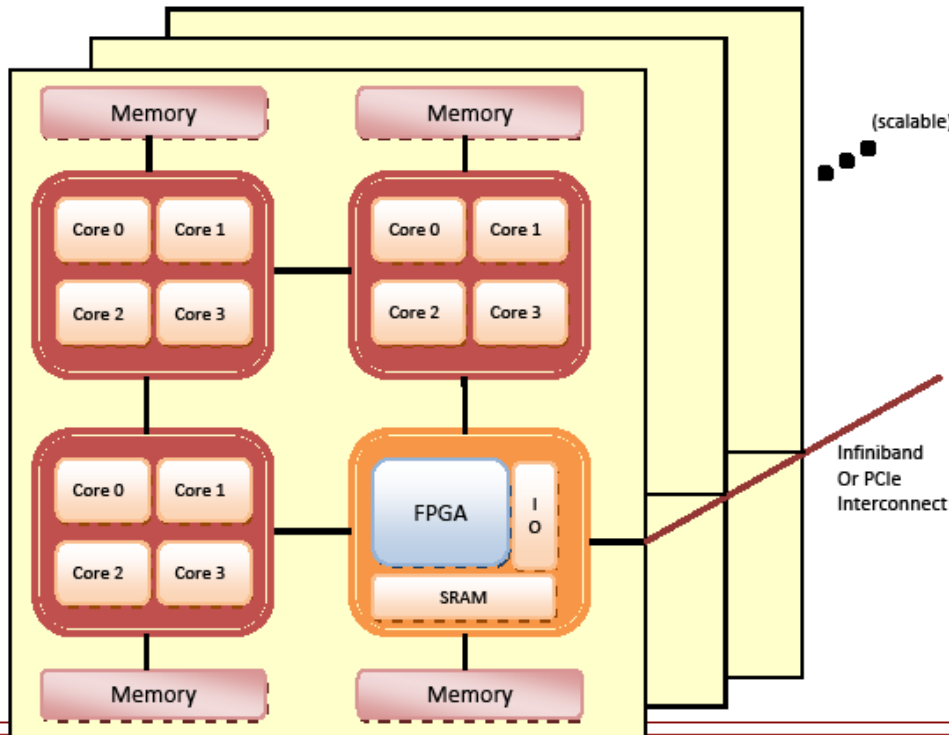
Reproduced with permission from: <http://ppl.stanford.edu/wiki/images/9/93/PPL.pdf>



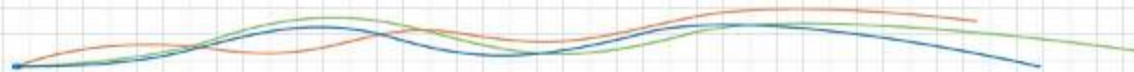


Stanford FARM: Flexible Architecture Research Machine

FARM: Flexible Architecture Research Machine



- Commodity CPUs and FPGAs in memory system
- Scales as needed



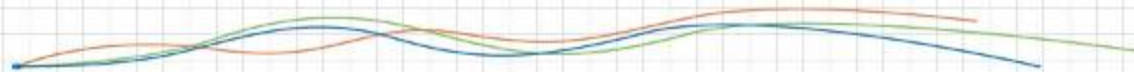


FARM: Many Possibilities



- **FPGA provides great environment for evaluating architectural ideas at full system speed**
 - Accelerators: video encoding, encryption, ISA extensions, etc.
 - Heterogeneous architectures
 - Simple cores on FPGA
 - Hardware schedulers
 - Maintain rich software support via OS, etc.
- **Platform with high bandwidth, low latency, coherent link to FPGA**
 - Great for FPGA-based simulators in RAMP

- **Potential Procyon Research Areas**
 - **Transactional Memory**
 - **New Processor Architectures**
 - **Compute Acceleration Algorithms**
 - **Application Specific Co-Processors**
 - **High Speed Interconnect**





Single Board Computer

- AD7003 Procyon SBC with AMD Opteron Processor

Calculation Accelerator

- AD7003-01 CPU Co-Processor Board with AMD Opteron Processor
- AD5440-xx FPGA Co-Processor Board

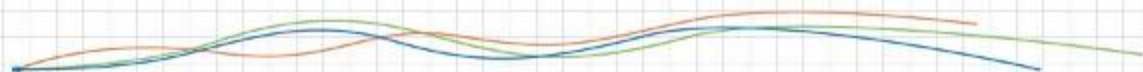
Hyper Transport I/O Boards

- AD5440-HT01 Engine HIL Board
- AD5440-HT02 Motor HIL Board
(support electrical JMAG motor model under consideration)
- AD5440-HT11 PWM/Digital I/O Board



PCIe I/O Boards

- AD5440-PX04 1.25MHz-Sampling/12ch Combustion Analysis Board
- AD5440-PX06 NVH Analysis Board

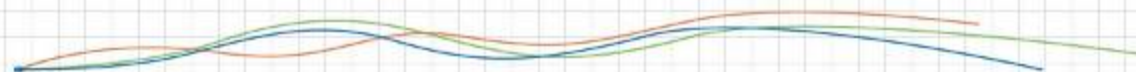




cPCI I/O Boards (Compact PCI Base)

CompactPCI®

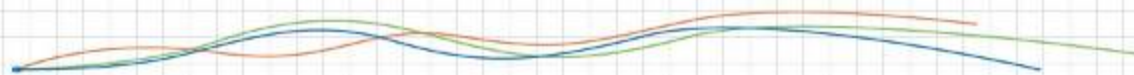
- AD5440-01 32ch Analog Input Board
- AD5440-02 32ch Analog Output Board
- AD5440-03 Digital I/O Board (Flex-channel)
- AD5440-06 Multifunction I/O Board (A/D12ch, D/A8ch, DI 16ch, DO 16ch)
- AD5440-08 Servo Controller (4ch Input/1ch Output)
- AD5440-09 8ch Strain Gauge Input Board (Simultaneous Sampling)
- AD5440-10 Box-to-Box Synchronization Board
- AD5440-11 PWM I/O Board
- AD5440-15 Box-to-Box Communication Board
- AD5440-17 Network Board (CAN, Serial, K-Line, Lin)
- AD5440-20 16ch/250kHz Analog Input Board (Simultaneous Sampling)



Collaboration Plan



- Open Specification
 - Enables 3rd-party Peripheral board development
- Development Environment Kit
 - SBC (Castor)
 - Backplane (Leda)
 - HyperTransport and PCI Express Evaluation I/O Board (Pollux)
- Software Environment
 - Standard x86 platform
 - Real-time OS Available
 - Supports The MathWorks MATLAB/Simulink
 - Application Design Environment (VirtualConsole)
 - Support 3rd-party Software Execution (Vehicle model, Engine model, etc.)



Thank you for your attention



Contact: procyon@aanddtech.com

