HTCE Symposium 2009
Program

SYMPOSIUM
Wednesday, Feb. 11th

	08:00	**-**	**09:00**	**Registration**
Morning Session	**09:00**	**-**	**09:30**	**Welcome Address and Update on HTCE's work** *Prof. Ulrich Brüning, University of Heidelberg & HTCE*
	09:30	**-**	**10:00**	**HyperTransport - Extending Technology Leadership** *Mario Cavalli, General Manager at HyperTransport Technology Consortium*
	10:00	**-**	**10:30**	**Coffee Break**
	10:30	**-**	**11:00**	**Open Source Business Models** *Monty Widenius, MySQL Founder*
	11:00	**-**	**11:30**	**System Impact of Integrated Interconnects** *Prof. Sudhakar Yalamanchili, Georgia Institute of Technology*
	11:30	**-**	**12:15**	**Guided Lab Tour**
	12:30	**-**	**13:30**	**Lunch at the Cafeteria**
Afternoon Session	**13:45**	**-**	**15:15**	**Technical Session I** 13:45 Building blocks for custom HyperTransport solutions *Holger Fröning, University of Heidelberg & HTCE* 14:15 Maintaining Cache Coherency with AMD Opterons using FPGAs *Parag Beeraka, AMD* 14:45 Scalable OpenMP Programming *Dieter an Mey & Christian Terboven, RWTH Aachen*
	15:15	**-**	**15:45**	**Coffee Break**
	15:45	**-**	**16:45**	**Technical Session II** 15:45 Leveraging HyperTransport for a custom high-performance cluster network *Mondrian Nüssle, University of Heidelberg & HTCE* 16:15 Procyon - The ultra-high-performance simulation and control platform with HyperTransport, *Satoshi Furukawa, A & D Technology*
	17:00	**-**	**17:30**	**HyperTransport Technology in 2009 and beyond (presented by video conference)** *Mike Uhler,Vice President, Accelerated Computing, AMD*
	17:30	**-**	**17:45**	**Closing remarks** *Prof. Ulrich Brüning, University of Heidelberg & HTCE*
	18:30	**-**	**23:00**	**Social Event** at the Museum Paddle Steamer Mannheim Reception, guided demonstration of the steam machine & dinner

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WORKSHOP
Thursday, Feb. 12th

Key Note	**09:00**	**-**	**10:00**	**Beyond the power and memory walls: The role of HyperTransport in future system architectures** *Prof. José Duato, Universidad Politècnica de Valencia*
Morning Session	**10:00**	**-**	**10:35**	**Workshop Papers I** 10:00 PGAS Model for the Implementation of Scalable Cluster Systems *Juan A. Villar, Francisco Andújar, Francisco J. Alfaro, José L. Sánchez, José Duato*
	10:40	**-**	**11:10**	**Coffee Break**
	11:10	**-**	**12:20**	**Workshop Papers II** 11:10 Exploiting the HTX-Board as a Coprocessor for Exact Arithmetics *Fabian Nowak, Rainer Buchty, David Kramer, Wolfgang Karl* 11:45 HyperTransport 3 Core: A Next Generation Host Interface with Extremely High Bandwidth *Benjamin Kalisch, Alexander Giese, Heiner Litz, Ulrich Brüning*
	12:30	**-**	**13:30**	**Lunch at the Cafeteria**
Afternoon Session	**13:45**	**-**	**14:55**	**Workshop Papers III** 13:45 Run-Time Reconfiguration for HyperTransport coupled FPGAs using ACCFS *Jochen Strunk, Andreas Heinig, Toni Volkmer, Wolfgang Rehm and Heiko Schick* 14:20 A general purpose HyperTransport-based Application Accelerator Framework *David Kramer, Thorsten Vogel, Rainer Buchty, Fabian Nowak and Wolfgang Karl*
	15:00	**-**	**15:30**	**Coffee Break**
	15:30	**-**	**16:40**	**Workshop Papers IV** 15:30 Extending HyperTransport Protocol for Improved Scalability *J. Duato, F. Silla, B. Holden, P. Miranda, J. Underhill, M. Cavalli, S. Yalamanchili and U. Brüning* 16:05 A HyperTransport-Enabled Global Memory Model For Improved Memory Efficiency *Jeffrey Young, Sudhakar Yalamanchili, Federico Silla and Jose Duato*
	16:45	**-**	**17:00**	**Closing remarks** *Prof. Ulrich Brüning, University of Heidelberg & HTCE*