Research Project: BigIron2

Large Scale Coherent Shared Memory Systems for In-Memory Computing

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Motivation



- We need to innovate without disrupting. (Like your multicore laptops.)
- Large memory technology is poised to take off, and it needs appropriate hardware.
- High Performance Computing (HPC) has yielded results that can now be applied to Enterprise Software.
- We have a lot of cores now and better interconnects.
- We can "flatten" the layers and simplify.
- We can build systems that improve our software *now* without making *any* modifications.
- Nail Soup argument: But, if we are willing to modify our software, we can win bigger. But we do this on our own schedule.



Real real-time computing is possible because of in-memory computing

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In Memory Computing





In-Memory Computing

Technology that allows the processing of **massive quantities of real time data** in main memory to provide real time decision making and analytics.

SAP Products With In-Memory Computing Introducing SAP High Performance Analytic Appliance (HANA)

Real Real-time

- Sub-second update latency
- No materialized views

Fast

- Native multi-core & MMP support
- Full featured in-proc calc engine
- "BWA on steroids"

Simple & Easy

- Pre-configured appliance
- Modeling based on SBO Information Designer ("universe")
- Packaged SAP content

Open

- Full ANSI 92 SQL
- MDX



BigIron2 is the second system on a path toward costeffective, high performance in-memory computing



Coherent shared memory (CSM)



Provides the ability to build a scalable SMP (Symmetric Multi-Processor) system with a uniform and coherent memory addressing architecture that can scale to 10's of terabytes of directly accessible, random access, primary memory. CSM is also called Cache Coherent Non-Uniform Memory Access (ccNUMA).





Taking In-Memory Computing Seriously



Basic Assumptions and observations

- Hard disks are for archives only. All active data must be in DRAM memory.
- Data locality is essential. Otherwise CPUs are stalled due to too many cache misses
- There are many levels of caches
- Problems and Opportunities for In-Memory Computing
 - Addressable DRAM per box is limited due to processor physical address pins.

- But we need to scale memory independently from physical boxes

- Scaling Architecture
 - Arbitrary scaling of the amount of data stored in DRAM
 - Arbitrary and independent scaling of the number of active users and associated computing load
- DRAM access times have been the limiting factor for remote communications
 - Adjust the architecture to DRAM latencies (<100 ns?)
 - InterProcess Communication is slow and hard to program (latencies are in the area of 0.5-1ms)

Coherent Shared Memory – The Alternative to Remote Communication

SAP

- Uses high-speed, low latency networks (Optical copper/fiber with 40Gb/s or above)
 - Typical latencies of this are in the area of 1-5 µsec
 - Throughput is higher than the CPU can consume
 - L4 cache needed to balance the longer latency on non-local access (cache-coherent non-uniform memory access over different physical machines)
- Separate the data transport and cache layers into a separate tier below the operating system- never seen by the application or the operating system!
- Applications and database code can just reference data
 - The data is just "there", i.e. it's a load/store architecture, not network datagrams
 - Application level caches are possibly not necessary the system does this for you.
 - Streaming of query results is simplified, L4 cache schedules the read operations for you.
 - Communication is much lighter weight. Data is accessed directly and thread calls are simple and fast (higher quality by less code)
 - Application designers do not confront communications protocol design issues
 - Parallelization of analytics and combining simulation with data are far simpler, enabling powerful new business capabilities of mixed analytics and decision support at scale

Implications of Coherent Shared Memory



- Access to database can be "by reference"
- No caches on application server side. Application can refer to database query results including metadata, master data etc. within the database process.
- Caches are handled by "hardware" and are guaranteed to be coherent.
- Lean and fast application server for in-memory computing
- On Database Code
 - A physically distributed database can have consistent DRAM-like latencies
 - Database programmers can focus on database problems
 - Data replication and sharding are handled by touching the data and L4 cache does the automatic distribution
- In fact, do we need to separate application servers from database servers at all?
- No lock-in to fixed machine configurations or clock rates
- No need to make app-level design tradeoffs between communications and memory access

But what about...



- Distributed Transactions?
 - We don't need no stinkin' distributed transactions!
- What about traditional relational databases?
 - In the future, databases become data structures!
- Well, not really. Just wanted to make the point. (grant me some poetic license here)
- Is it Virtualization?
 - In traditional virtualization, you take multiple virtual machines and multiplex them onto the same physical hardware. We're taking physical hardware instances and running them on a single virtual instance.
- Why not build a mainframe?
 - It is a mainframe

The business benefits of coherent shared memory



Improved in-memory computing performance at dramatically lower cost

- The ability to build high performance "mainframe-like" computing systems with commodity cluster server components
- Ability to scale memory capacity in a more in-memory computing-friendly fashion
- Simplified software system landscape using system architecture that can be made invisible to application software

Minimize changes to SAP applications

- Enables SAP applications to scale seamlessly without changes to the application code or additional programming effort
- With coherent shared memory, the bulk of SAP's developers can develop as they do today and let the underlying hardware and lower level software handle some of the resource allocation, unlike today.

A simpler programming model



Before



Sufficiently skilled programmers will be scarce



After

- Initial design is timeless hardware scaling handled below app design layer
- Developers do not need additional skills for in-memory computing

Hardware and software approaches to coherent shared memory



Hardware Approaches





Custom and proprietary chipsets (e.g. NumaChip in diagram), with software and commodity interconnects such as InfiniBand, aggregate compute, memory and I/O capabilities of each system



Hardware approach is replicated in software
Software aggregates the compute, memory, and I/O capabilities of each system and presents a unified virtual system to both the OS and the applications running above the OS via a software interception engine

Multiple companies are developing and/or delivering relevant solutions



Processor Companies Hardware and Software Solutions Via 3 Leaf Systems acquisition – HyperTransport approach **ScaleMP** Start-up with software-based approach - vSMP numasca Start-up with SMP adapter card Hardware-based node-controller solution Sgi Hardware-based node-controller solution

HyperTransport HyperTransport extensions **QPI** (Quick Path Interconnect) Technology extensions

BigIron 2: The system we have architected and built via leading-edge, standard, cluster server components



Big Iron 2 Extreme Performance, Scalability, and much simpler system model **System Specifications** Architecture, **Research Server Cluster** Assembly, 5 x 4U Servers System architecture: SAP Technology SAP VPN swh/rtr (4 Intel XEON x7560 2.26Ghz) Infrastructure 160 cores (32 Cores/Server) SAP 1Gb swh **Research Practice 5TB memory** (64 x 16MB + 36 TB DDR3/Server) Assembly and Test: Colfax 30TB SSD (solid state disk) International + 36 TB storage Hosting: **Bav Area Internet** 5 Networks + 36 TB Solutions, Santa VPN of ScaleMP (40-Clara, CA 160GbIB) + 36 TB VPN of Server Cluster NAS 36 TB (10GbE) VPN of Storage Array 10Gb swh (10GbE) **KVM** VPN of SAP Internal Network 40Gb IB swh (10MbE metered) Biglron2-05 Firewalled GW to Internet • Large shared (1GbE Expandable) coherent Biglron2-04 I NAS (72TB Expandable to 180) memory 1 x 48U Rack (5TB) across Biglron2-03 Svstem Software servers via SLES11 Linux OS Licenses Scale MP Biglron2-02 ScaleMP vSMP Licenses • 160 Lower System cost cores(320 Biglron2-01 HT)

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Open Research Questions



- What is the most applicable and realistic approach for SAP? (e.g. in hardware vs. in software)
- Is a software approach even feasible given long-range hardware capabilities and performance estimates?
- What is the right size of L4 cache? What are the working sets? Managing all cache levels.
- What are the interconnect options and latency characteristics. Tradeoffs?
- Are fewer faster sockets/board better than more sockets?
- What are the operational issues, including DB load, errors, failover, resiliency, scale, etc.

Sample BI2 Performance Matrix





Sample BI2 Performance Matrix





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1-3 years

Market

Questions?

