The FSM Designer4

a high-level design entry tool

Description

The FSMDesigner4 is an application for interactive design and specification of finite state machines (FSMs) and automatic generation of their hardware description language (HDL) implementation. The graphical representation of a FSM also serves as documentation. This application is implemented especially for designing fast complex control circuits. Therefore a simple Moore Machine is selected as a reasonable design target for FSMs. The FSMDesigner4 provides an intuitive and time efficient way to design such FSMs. Thereby this application is saving design time (“time to market”), which becomes increasingly important while complexity of control circuits increases. A high usability is guaranteed by non-modal widgets, context menus, table-based editing, and common application functionalities. Thus not only designing a FSM, but also upgrading or adapting FSMs becomes efficient. Portability is granted by using a well defined extensible markup language (XML) format for saving FSMs. It is human readable and defined regarding to the official standards for XML.

The FSMDesigner4 application is able to generate Verilog HDL 2001 compatible code. The application is written in C++ with the use of Trolltech’s Qt4 to implement a graphical user interface (GUI). The development environment is Linux. Thus a version for Linux is already available. Portability to other operating systems should easily be possible.

Features:

- Complete graphical design of finite state machines including:
  - states, transitions, conditions
  - links, joins
  - hierarchies and global transitions
- Modern GUI with commonly expected functionalities as:
  - multiple redo, undo, etc.
- Save & load functionality in well defined XML-files guarantees high portability for further use
- Validation of FSMs
- Minimization functionality to optimize selected transitions
- Generation of optimized RTL HDL output (currently Verilog)
- Default transition support (xrest-function)
- Fully scriptable with TCL or Python
- Verification is supported by an interface for simulation of FSMs
- Easy and fast table based data manipulation

University of Mannheim
Computer Architecture Group
Prof. Dr.-Ing. Ulrich Brüning
Tel. +49 621 181 2723 Fax +49 621 181 2713
http://www.ra.ti.uni-mannheim.de