CAG HT3 VIP Overview

1 Introduction

The CAG HT3 Verification IP(VIP) is an Open Verification Component (OVC) for modern coherent Hypertransport 3 cores. It is written completely in SystemVerilog. The OVC follows the Open Verification Methodology (OVM) for verification components, which was introduced by Mentor Graphics and Cadence.

The CAG HT3 OVC was developed to overcome some drawbacks of the existing (non-)coherent HT3 BFM from AMD. The AMD BFM is a standard Verilog BFM. It consists of a Verilog wrapper and a core model written in C. As such it does not fit very well in a modern verification environment. The AMD BFM also has no support for coverage sampling, which is crucial for a complete verification environment. The last point for not using the BFM is the fact that AMD has stopped the development of the BFM. At the moment there are some known bugs inside the BFM, which will not be fixed in the near future.

The goal of this development was to have an easy to use (non-)coherent HT3 layer for system level verification environments on the one hand and reuse the HT3 OVC in a module level verification environment for the CAG HT3-core on the other hand.

The HT3 OVC currently implements the following features:

- HT generation 1 and generation 3 operation mode
- Link widths of 8-bit and 16-bit
- Link initialization (gen1/gen3)
- Credit handling
- Periodic CRC insertion
- Command packet insertion
- Acknowledge handling in gen3 operation
- Link scrambling in gen3 operation
- Sending and receiving of all defined (n)cHT3 packets
- Retry mode
- Link disconnect and reconnect sequence

2 OVC Description

The HT3 Verification environment consists of two main OVCs as shown in figure 1. The HT OVC and the HT App OVC. The HT OVC handles the HT3 link protocol. As such it is connected to the link interface of the HT3 core. The HT App OVC connects to the application buffers of the HT3 core.

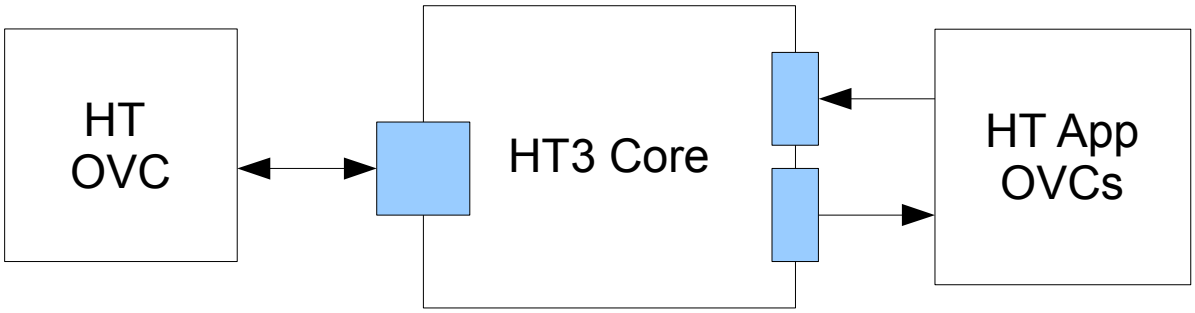

Figure 1: HT3 Verification Environment

3 The HT OVC

The HT OVC (*figure 2*) consists of a sequencer, a driver, two monitors and a global configuration. It can be configured to operate in active or passive mode. As it follows the OVM guideline, it can be easily integrated into system level verification environments as an interface OVC. Module OVCs can access the HT OVC by the OVM OVC layering mechanisms.

The HT OVC implements the whole HT 3.1 specification.

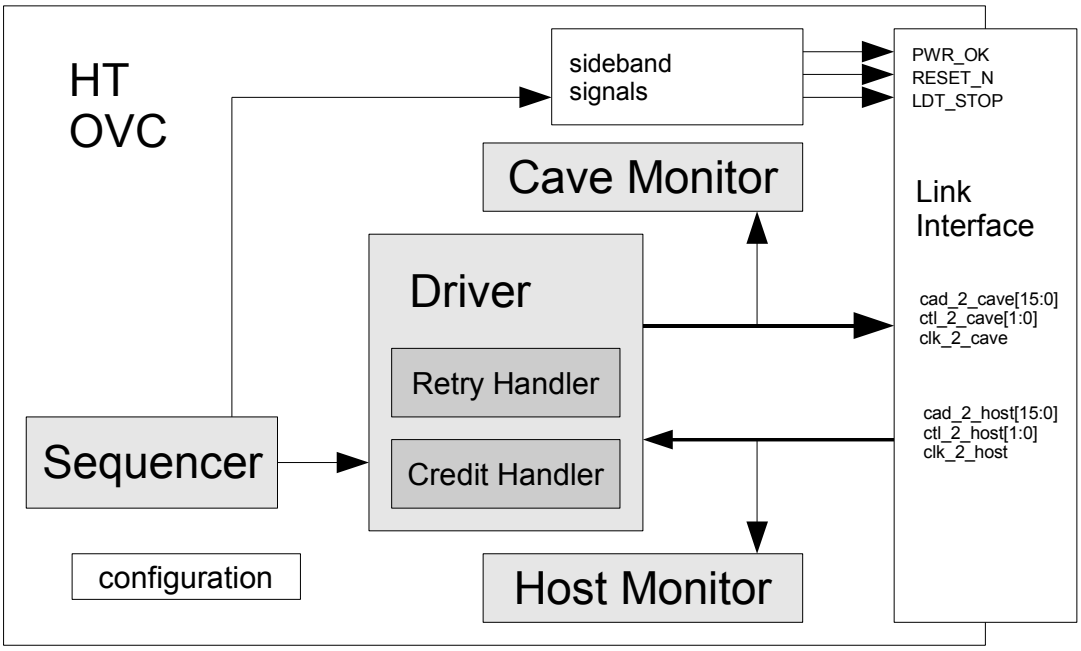

Figure 2: The HT OVC