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HyperTransport 3.0 Link Core IP

Executive Summary:
The HyperTransport 3.0c Link Core IP implements the HyperTransport host bus interface and bridges it to a deserialized and decoded parallel user interface. Implemented in a device, the link core allows to directly connect to AMD Opteron processors through a coherent an non coherent HyperTransport link. The link core enables tightly coupled, high bandwidth and low latency systems. The link core IP implements the physical and the link layer of HyperTransport including SERDES, flow control, virtual channel management, fault tolerance and data packetization.

Features:

- Fully HyperTransport 3.0c compliant
- The following link frequencies are supported: HT200, HT400, HT600, HT1000, HT1200, HT1600, HT1800, HT2000, HT2400, HT2600
- Support of 8 and 16 bit links
- Peak theoretical bidirectional bandwidth of 20.8 GByte/s
- Unidirectional latency below 30ns
- Coherent and non coherent version available
- Synchronous and asynchronous mode
- 650 MHz core frequency at HT2600
- Independent fifo based 128 bit user interface for each virtual channel (posted, non posted, response)
- TSMC 65nm technology
- FPGA ports available for Xilinx and Altera
- OVM verification environment and bus functional model available
- Gate count: 123.000

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