The Xilinx UltraScale Architecture

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FPGA Basics

FPGA Generations and Examples
   Xilinx Virtex-7
   Altera Stratix 10

The Xilinx UltraScale Architecture
   Foundation for Success
   Market Requirements
   Device Portfolio
   Features
   Applications

Evaluation

Summary and Conclusion
Field-Programmable Gate Array

General-purpose semiconductor device

Programmed after manufacturing

Opposite: ASIC, ASSP, etc.
  - Application-specific
  - predefined HW function

Applications: Audio, Security, Video/Imaging

Markets: Automotive, Aerospace/Defense, Broadcast, Consumer Electronics, Medical, Wireless/Wired Communication

Figure 1: Nexys 3 Spartan-6 FPGA Board [1]
Building Blocks

- CLBs/LEs
- I/O
- Interconnect
- Special Functions:
  - Memory
  - DSP
  - Serial Transceivers
  - Clocking

**Figure 2: FPGA Structure [5]**

[2–4, 6–11]
Figure 3: Spartan-6 FPGA Architecture [12]

Figure 4: Functionality of a SerDes [13]
FPGA Generations

• Low-Cost: Spartan/Artix, Cyclone
• Mid-Range: Kintex, Arria
• High-End: Virtex, Stratix

Figure 5: FPGA Generations [14–22]
Example 1: Xilinx Virtex-7 Architecture

- **28nm HKMG** HPL process technology
- **Unified architecture** in whole 7 series:
  - AMBA AXI interconnect standard
  - ASMBL architecture

*Figure 6: Comparison of Standard and HKMG Transistors [35]*

*Figure 7: The ASMBL Architecture [40]*
Example 1: Xilinx Virtex-7
Performance and Power

- **2x system performance** or 50% lower **power**: up to 600 MHz or less than 2 W
- **1.8x DSP** performance: up to 5,335 GMAC/s, up to 3,600 DSP Slices

- **1.6x I/O bandwidth**: up to 2,784 Gb/s, up to 96 high-speed serial transceivers
- **2x memory bandwidth**: 1,866 Mb/s (DDR3)
- **2x density**: almost 2 million logic cells

*Figure 8: Performance and Power Consumption Compared to Last-Generation Devices [26]*
Example 2: Altera’s Stratix 10 FPGA Architecture

- **Figure 9**: Effective Channel Widths of Planar and TriGate Transistor Structures

  - Intel **14-nm **TriGate** process technology
  - **HyperFlex** architecture
  - Heterogeneous 3D solutions possible

  [18, 44–50]
Example 2: Altera’s Stratix 10 FPGA

Performance and Power

- **2x core** performance (> 1GHz) or up to 70% less power

- **DSP** performance: > 10 TFLOP/s at 100 GFLOPs/W

- **4x transceiver** bandwidth (up to 8,064 Gb/s, up to 144 transceivers)

- **Memory** bandwidth: e.g. DDR4 at 3,200 MB/s

- **Largest** monolithic FPGA: > 4 million logic elements

*Figure 10: Stratix 10 Performance [46]*

[18, 44–49]
The 7 Series as "Foundation for Success"

Silicon Process Technology
- partnership with TSMC

Generations:
1. 28\textit{nm} HPL
2. 20\textit{nm} 20SoC planar
3. 16\textit{nm} FinFET

Stacked Silicon Interconnect (SSI) Technology
- 3D ICs

Generations:
1. 7 series
2. UltraScale

Vivado Design Suite
- better design placement and routing
- improved software runtime
- co-optimization with devices

[37, 51–55]
Market Requirements

Resulting from the "More is Better Mindset"

Figure 11: High-Performance Systems Require Massive Bandwidth [52, p. 9]
### Device Portfolio

<table>
<thead>
<tr>
<th>Maximum Capability</th>
<th>Kintex UltraScale</th>
<th>Virtex UltraScale</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Introduction Shipment</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Process Technology</strong></td>
<td>20nm planar</td>
<td>20nm planar, 16nm FinFET</td>
</tr>
<tr>
<td><strong>Logic Cells</strong></td>
<td>1,160K</td>
<td>4,407K</td>
</tr>
<tr>
<td><strong>Block RAM</strong></td>
<td>76Mb</td>
<td>115Mb</td>
</tr>
<tr>
<td><strong>DSP48 Slices</strong></td>
<td>5,520</td>
<td>2,880</td>
</tr>
<tr>
<td><strong>Peak DSP Performance</strong></td>
<td>8,180 GMAC/s</td>
<td>4,268 GMAC/s</td>
</tr>
<tr>
<td><strong>Transceivers</strong></td>
<td>64</td>
<td>104</td>
</tr>
<tr>
<td><strong>Peak Transceiver Speed</strong></td>
<td>13.6 Gb/s</td>
<td>32.75 Gb/s</td>
</tr>
<tr>
<td><strong>Peak Serial Bandwidth</strong></td>
<td>2,086 Gb/s</td>
<td>5,101 Gb/s</td>
</tr>
<tr>
<td><strong>PCIe Blocks</strong></td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td><strong>100G Ethernet Blocks</strong></td>
<td>2</td>
<td>7</td>
</tr>
<tr>
<td><strong>150G Interlaken Blocks</strong></td>
<td>1</td>
<td>9</td>
</tr>
<tr>
<td><strong>Memory Interface</strong></td>
<td></td>
<td>2,400 Mb/s</td>
</tr>
<tr>
<td><strong>I/O Pins</strong></td>
<td>832</td>
<td>1,456</td>
</tr>
</tbody>
</table>

Specialization: Signal Processing, Processing, Bandwidth, Throughput

[38, 51, 53, 56–58]
Features: Scalability

Across the Platform

- **7 series**: same lowest-level building blocks in different FPGA families
- **UltraScale**: additional package footprint capability across Virtex and Kintex families

From 20nm Planar to 16nm FinFET

*Figure 12*: Scalability within the Xilinx FPGA Portfolio [59]
Features: Data Flow and Routing

Figure 13: The Effect of Fast Tracks on Routing: More Interconnect Tracks [54]

⇒ over 90% utilization

[30, 51, 53, 54]
I/O Bandwidth
- high-speed serial transceiver (GTY, GTH)
- internal gearbox logic

Memory Bandwidth
- SDRAM: more controllers, wider and faster ports
- hardened SDRAM PHY blocks
- BRAM and FIFO improvements

DSP Processing
- 27x18-bit multipliers
- non-DSP computations possible

Packet Processing
- modified DSP slices
- hardened Gigabit Ethernet MACs and Interlaken chip-to-chip interfaces

[30, 51, 53, 54, 60–67]
Other Features

Figure 14: Other Features of the UltraScale Architecture

[30, 51, 53, 54, 68–70]
Applications

Figure 15: Example Application of the UltraScale Architecture in Digital Video Processing [54, p. 15]

[30, 54, 71, 72]
### Evaluation

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<tr>
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<th>Virtex-7</th>
<th>Kintex UltraScale</th>
<th>Virtex UltraScale</th>
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<tbody>
<tr>
<td>Introd./Shipm.</td>
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<td>2013/2014</td>
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<tr>
<td>Process Technology</td>
<td>28nm planar</td>
<td>20nm planar</td>
<td>20nm planar, 16nm FinFET</td>
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<td>Logic Cells</td>
<td>1,955K</td>
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<tr>
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<td>68Mb</td>
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<td>3,600</td>
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<tr>
<td>Peak DSP Performance</td>
<td>5,335GMAC/s(^1)</td>
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<tr>
<td>Transceivers</td>
<td>96</td>
<td>64</td>
<td>104</td>
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<tr>
<td>Peak Transceiver Speed</td>
<td>28.05Gb/s</td>
<td>13.6Gb/s</td>
<td>32.75Gb/s</td>
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<tr>
<td>Peak Transceiver Bandwidth</td>
<td>2,784Gb/s(^3)</td>
<td>2,086Gb/s(^3)</td>
<td>5,101Gb/s(^3)</td>
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<tr>
<td>PCIe Blocks(^4)</td>
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<td>6</td>
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<td>100G Ethernet</td>
<td>0</td>
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<td>1,866Mb/s</td>
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Specialization: Overall Performance, Signal Processing

\[^1\] based on symmetrical filter implementation

\[^2\] single-precision, hardened floating point DSP performance

\[^3\] Full Duplex

\[^4\] x8 Gen3

\[^5\] Virtex-7: DDR3, UltraScale: DDR4
## Evaluation

### Current Generation Devices

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<td>1, 160K</td>
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<td>&gt; 4, 000K</td>
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<td>DSP Slices</td>
<td>5, 520</td>
<td>2, 880</td>
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<td>DSP Performance</td>
<td>8, 180GMAC/s¹</td>
<td>4, 268GMAC/s¹</td>
<td>&gt; 10,000GFLOP/s²²</td>
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<td>104</td>
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<td>8, 064Gb/s</td>
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1. based on symmetrical filter implementation
2. single-precision, hardened floating point DSP performance
3. Full Duplex
4. x8 Gen3
5. DDR4

[18, 38, 44–49, 51, 53, 56–58]
Summary

- "More is better Mindset"
- Kintex UltraScale, Virtex UltraScale
- 2nd generation 3D ICs
- Improvements on former bottlenecks (i.e. interconnect)
- Special Features (e.g. ASIC-like clocking)

Conclusion

- Specialization
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  - Overall performance (Virtex UltraScale)
- Poorer performance than competition, but already available
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⇒ Final Evaluation not until Stratix 10 is available!
Appendix

6 Additional Material
   Evaluation Details
   Application Example

7 References
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<td>Signal Processing</td>
<td>Overall Performance</td>
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¹ based on symmetrical filter implementation
² single-precision, hardened floating point DSP performance
³ Full Duplex
⁴ Virtex-7: DDR3, others: DDR4
Applications
Super Hi-Vision Camera

Figure 16: Example Application: Super Hi-Vision Camera [73]


References


References


